Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-15: Currently Cancelled.

16. (Currently Amended) A ~~[The]~~ method ~~[of claim 5, further]~~ comprising:

interconnecting a compute node with a shared memory node;

translating a processor instruction into an interconnect command, wherein translating the processor instruction into the interconnect command includes translating a processor store instruction into an interconnect write command;

transforming the interconnect command into a direct memory access interconnect command;

transmitting the direct memory access interconnect command via a link medium;

performing an operation defined by the direct memory access interconnect command;

receiving a write interconnect command from a host;

buffering a data;

reporting to the host that write interconnect command has been performed;

holding the data for a period of time; and

requesting that the host retry the write command at a later time.

17. (Currently Amended) A ~~[The]~~ method ~~[of claim 5, further]~~ comprising:

interconnecting a compute node with a shared memory node;

translating a processor instruction into an interconnect command, wherein translating the processor instruction into the interconnect command includes translating a processor store instruction into an interconnect write command;

transforming the interconnect command into a direct memory access interconnect command;

transmitting the direct memory access interconnect command via a link medium;

performing an operation defined by the direct memory access interconnect command; and

combining a plurality of interconnect write commands into a single direct memory access interconnect write command of a plurality of data elements.

18. (Currently Amended) A ~~[The]~~ method ~~[of claim 1,]~~ comprising:

interconnecting a compute node with a shared memory node;

translating a processor instruction into an interconnect command;

transforming the interconnect command into a direct memory access interconnect command;

transmitting the direct memory access interconnect command via a link medium; and

performing an operation defined by the direct memory access interconnect command;

wherein the shared memory node modifies a memory address statically.

19. (Currently Amended) A ~~[The]~~ method ~~[of claim 4, further]~~ comprising:

interconnecting a compute node with a shared memory node;

translating a processor instruction into an interconnect command;

transforming the interconnect command into a direct memory access interconnect command;

transmitting the direct memory access interconnect command via a link medium; and

performing an operation defined by the direct memory access interconnect command;

wherein transforming the interconnect command into the direct memory access interconnect command includes transforming the interconnect read command into a direct memory access interconnect read command; and

prefetching data with the compute node after translating the processor load instruction into the direct memory access interconnect read command.

20. (Original) The method of claim 19, wherein prefetching includes:

recording characteristics of a series of load instructions;

analyzing characteristics of the series of load instructions;

determining a pattern in the series of load instructions; and

speculatively issuing direct memory access interconnect read commands to the shared memory node as a function of the pattern.

Claims 21-28: Currently Cancelled.

29. (Currently Amended) An ~~[The]~~ apparatus ~~[of claim 27,]~~ comprising:

a computer network, including:

a compute node, having:

a compute node interconnect interface unit; and

a compute node interconnect adapter;

a link medium, coupled to the compute node; and

a shared memory node, coupled to the link medium, having:

a shared memory node interconnect interface unit; and

a shared memory node interconnect adapter;

wherein the compute node interconnect interface unit includes:

a processor bus;

a memory bus;

an interconnect bus;

a memory command translator; and

a memory address translator;

wherein the memory address translator includes a table of memory address ranges.

30. (Original) The apparatus of claim 29, wherein, wherein the table of memory address ranges includes a plurality of ranges associated with the interconnect bus.

31. (Original) The apparatus of claim 29, wherein the table of memory address ranges includes a plurality of ranges associated with the memory bus.

32. (Original) The apparatus of claim 29, wherein the table of memory address ranges is dynamically adjusted, with ranges determined at initialization time via a standardized test.

33. (Original) The apparatus of claim 32, wherein the standardized test includes reads and writes to certain required memory ranges within the compute node interconnect adapter.

34. (Currently Amended) An ~~[The]~~ apparatus ~~[of claim 28,]~~ comprising:

a computer network, including:

a compute node, having:

a compute node interconnect interface unit; and

a compute node interconnect adapter;

a link medium, coupled to the compute node; and

a shared memory node, coupled to the link medium, having:

a shared memory node interconnect interface unit; and

a shared memory node interconnect adapter;

wherein the shared memory interconnect interface unit includes:

a processor bus;

a memory bus;

an interconnect bus;

a memory command translator; and

a memory address translator;

wherein the memory address translator includes a table of memory address ranges.

35. (Original) The apparatus of claim 34, wherein, wherein the table of memory address ranges includes a plurality of ranges associated with the interconnect bus.

36. (Original) The apparatus of claim 34, wherein the table of memory address ranges includes a plurality of ranges associated with the memory bus.

37. (Original) The apparatus of claim 34, wherein the table of memory address ranges is dynamically adjusted, with ranges determined at initialization time via a standardized test.

38. (Original) The apparatus of claim 37, wherein the standardized test includes reads and writes to certain required memory ranges within the shared memory node interconnect adapter.

39. (Currently Amended) An ~~[The]~~ apparatus ~~[of claim 22,]~~ comprising:

a computer network, including:

a compute node, having:

a compute node interconnect interface unit; and

a compute node interconnect adapter;

a link medium, coupled to the compute node; and

a shared memory node, coupled to the link medium, having:

a shared memory node interconnect interface unit; and

a shared memory node interconnect adapter;

wherein the compute node interface adapter includes:

an interconnect bus interface;

an address translator;

a speculative-read control register;

a DMA-read control register;

a link protocol generator;

a link protocol responder;

a receive buffer;

a speculative-and-DMA read control calculator; and

a speculative-read control exerciser.

40. (Currently Amended) An ~~[The]~~ apparatus ~~[of claim 22,]~~ comprising:

a computer network, including:

a compute node, having:

a compute node interconnect interface unit; and

a compute node interconnect adapter;

a link medium, coupled to the compute node; and

a shared memory node, coupled to the link medium, having:

a shared memory node interconnect interface unit; and

a shared memory node interconnect adapter;

wherein the shared memory node interconnect adapter, includes:

an interconnect bus interface;

an address translator;

an interconnect read/write state machine;

a link protocol generator; and

a link protocol responder.

41. (Original) The method of claim 20, wherein prefetching activation is performed via a link protocol responder.

42. (Original) The method of claim 41, wherein activation via the speculative read control register includes activation for a particular region of the shared memory node.

Claims 43-46: Currently Cancelled.